Paper No. 14

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JOHANNES H.A. BREKELMANS, HANS J. KUNZ,
and JOHANNES S. VROMANS

Appeal No. 2001-1871
Application No. 09/082,449

ON BRIEF

Before JERRY SMITH, LEVY, and BLANKENSHIP, Administrative Patent Judges.

BLANKENSHIP, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1-3 and 5-7.

We reverse.

BACKGROUND

The invention relates to calibration of an oscillator which is part of a phase locked loop (PLL). Claim 7 is reproduced below.

> 7. A method of calibrating an oscillator, which forms a part of a phase-locked loop for synchronizing the phase-locked loop's oscillator with a carrier (CA), the method comprising the steps of:
>
> measuring a frequency difference (dF) between a nominal frequency (Fnom) of the carrier (CA) and a frequency (Fosc) of the phase-locked loop's oscillator; and
>
> adjusting the frequency (Fosc) of the phase-locked loop's oscillator in accordance with the measured frequency difference (dF).

The examiner relies on the following references:

Mogi	4,305,157	Dec. 8, 1981
Toda et al. (Toda)	5,388,125	Feb. 7, 1995

Claim 7 stands rejected under 35 U.S.C. § 102 as being anticipated by Toda.

Claims 1-3, 5, and 6 stand rejected under 35 U.S.C. § 103 as being unpatentable over Toda and Mogi.

Claim 4 is objected to as depending from a rejected claim, but deemed allowable if rewritten in independent form.

Claims 8-10 have been withdrawn from consideration.

We refer to the Final Rejection (Paper No. 6) and the Examiner's Answer (Paper No. 11) for a statement of the examiner's position and to the Brief (Paper No. 10) and the Reply Brief (Paper No. 12) for appellants' position with respect to the claims which stand rejected.

OPINION

Appellants assert the section 102 rejection of claim 7 is in error because, inter alia, the oscillator which is part of phase-locked loop 27 in Toda is VCO 271 (Fig. 6), rather than oscillator 36 (Fig. 4), as contemplated by the rejection. (Brief at 5.) The examiner responds (Answer at 6) that the frequency provided to phase lock loop (PLL) 27, as shown in Figure 6 of the reference, comes from oscillator 36 of Figure 4. The examiner concludes that oscillator 36 is part of PLL 27.

However, we agree in substance with appellants' position. We do not consider an oscillator that generates an input (e.g., oscillator 36) to a system (e.g., PLL 27) to comprise part of the system. Moreover, Toda does not refer to oscillator 36 as part of PLL 27. While mere terminology in a reference is not necessarily determinative of how the disclosure may be interpreted by one skilled in the art, the examiner has provided no supporting evidence that Toda might be interpreted by the artisan as anything different from its express disclosure.

The rejection of claim 7 (Answer at 3) further asserts that Toda discloses a "frequency measurement circuit 31-32" (Fig. 4) and a "frequency adjustment circuit 13." However, as clearly shown in Figure 4, and further described at columns 5 through 7 of the reference, component extraction unit 31 and frequency counter 32 form part of frequency difference detection means 13. In any event, as appellants point out (Reply Brief at 4), instant claim 7 requires that a frequency difference is measured between a nominal frequency of the carrier and a frequency "of the phase-locked loop's oscillator."

We agree with the examiner to the extent that the "true" values of the second intermediate frequency signal (fL2) stored in table 34 may correspond to the claimed nominal frequency of the carrier. Toda col. 4, ll. 45-52; col. 5, ll. 30-42. However, whether the "phase-locked loop's oscillator" is taken to be reference oscillator 36, as submitted by the rejection, or taken to be VCO 271 (Fig. 6) in PLL 27 (Fig. 4), we do not find disclosure or suggestion where the frequency of either is measured and compared to the frequency values stored in table 34; i.e., that a frequency difference such as that claimed is to be measured.

Independent claims 1 and 6 contain versions of the features we find lacking in the rejection with respect to claim 7. The section 103 rejection relying on Toda in view of Mogi, however, appears to represent a shift in position when compared to the section 102 rejection over Toda. "Toda differs from the claimed invention in that the oscillator is included in the PLL." (Answer at 4.) Mogi is asserted to teach "that a reference oscillator can be incorporated in a PLL." (Id.)

However, neither the section 102 nor the section 103 rejection shows disclosure or suggestion of measuring a frequency difference between a nominal frequency of the carrier and a frequency of a phase-locked loop's oscillator, as required by claim 1 and claim 6.

We thus do not sustain the rejections of claims 1-3 and 5-7.

CONCLUSION

The rejections of claims 1-3 and 5-7 are reversed.

REVERSED

JERRY SMITH Administrative Patent Judge	)
STUART S. LEVY Administrative Patent Judge	) BOARD OF PATENT) APPEALS) AND) INTERFERENCES
HOWARD B. BLANKENSHIP Administrative Patent Judge	)

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